

DSR-14446



July 31, 2006

To: Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Fr: George O. Saile, Reg. No. 19,572
28 Davis Avenue
Poughkeepsie, NY 12603

Subject: | Serial No. 10/706,839 | 11/12/03 |

Taner Dosluoglu

VERTICAL CHARGE TRANSFER ACTIVE
PIXEL SENSOR

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Enclosed is Form PTO-1449, Information Disclosure Citation In An Application.

The following Patents and/or Publications are submitted to comply with the duty
of disclosure under CFR 1.97-1.99 and 37 CFR 1.56.

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States
Postal Service as first class mail in an envelope addressed to: Commissioner for Patents,
P.O. Box 1450, Alexandria, VA 22313-1450, on August 3, 2006.

Stephen B. Ackerman, Reg. # 37761

Signature/Date  8/3/06

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This Information Disclosure Statement is being filed after the mailing date of a Final Action under 1.113 or a Notice of Allowance under 1.311, whichever comes first, but before, or simultaneously with, the payment of the Issue Fee.

I hereby state that each item of information contained in this Information Disclosure Statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than 3 months prior to the filing of this statement.

The Commissioner is hereby authorized to charge the IDS Processing Fee of \$180, under 37 CFR 1.17(p), to Deposit Account No. 19-0033. A duplicate copy of this sheet is enclosed.

U.S. Patent 4,906,856 to Iwanami et al., "Semiconductive Photodetection Device Having Coplanar Circuit Components," discloses a photoelectric conversion array comprised of a longitudinal semiconductor substrate formed with a plurality of doped regions electrically isolated from one another and equidistantly aligned in the longitudinal direction of the substrate.

European Patent Application EP 1 469 521 A2 to Taner Dosluoglu et al., "CMOS Pixel Using Vertical Structure and Sub-Micron CMOS Process," describes a CMOS pixel responsive to different colors of optical radiation without the use of color filters.

U.S. Patent 6,023,293 to Watanabe et al., "Active Type Solid-State Imaging Device," discloses an active type solid-state imaging device where the image sensor portion and the driving circuit portion which drives the image sensor portion or conducts signal processing are formed in separate semiconductor regions in the identical semiconductor substrate.

A translation of the abstract of JP 56150878 is attached:

Patent Abstracts of Japan JP 56150878 to Tamamushi Naoshige, "Semiconductor Image Pickup Device," discusses improving the sensitivity and the resolution of a semiconductor image pickup device.

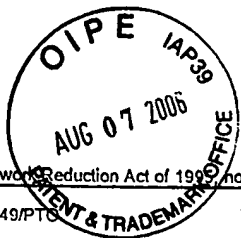
European Patent Application 0 400 153 A1 to Yano, "Optical Semiconductor Device Having a Zero-Crossing Function," discusses an optical semiconductor device having a zero-crossing function constituted by a light trigger thyristor controlled by a light trigger signal, a MOSFET and a Zener diode that are formed in the same semiconductor substrate in a monolithic form.

Sincerely,



Stephen B. Ackerman,
Reg. No. 37761

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PTO/SB/08B (07-05)

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Substitute for form 1449/PTO

**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

(Use as many sheets as necessary)

Complete if Known

Application Number

10/706,839

Filing Date

11/12/03

First Named Inventor

Tamer Desluoglu

Art Unit

Examiner Name

Sheet

of

Attorney Docket Number

DSR-14446

NON PATENT LITERATURE DOCUMENTS

Examiner Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²

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Signature

Date

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*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

¹ Applicant's unique citation designation number (optional). ² Applicant is to place a check mark here if English language Translation is attached.

This collection of information is required by 37 CFR 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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